SGS-THOMSON MICROELECTRONICS

ST1305

HIGH ENDURANCE CMOS 192 bit EEPROM WITH SECURE LOGIC ACCESS CONTROL

- SINGLE 5V SUPPLY VOLTAGE
- PROGRAMMING TIME: 5 ms
- MEMORY DIVIDED INTO:
  - 16 bits of Chip Data
  - 48 bits of Application Data
  - 48 bits of Count Data
  - 12 extra-bits of Transport Code
  - 64 bits of Issuer Data
- COUNTING CAPABILITY up to 262,144 UNITS
- CIRCUIT PROTECTED by TRANSPORT CODE for DELIVERY from SGS-THOMSON to the CUSTOMER
- 5 EXTERNAL CONTACTS ONLY (ISO 7816 COMPATIBLE)
- ANSWER to RESET FULLY COMPATIBLE with ISO 7816-3
- E.S.D. GREATER THAN 4000V
- POWER-ON and LOW V_{CC} RESET
- 10 YEARS DATA RETENTION
- 1 MILLION ERASE/WRITE CYCLES ENDURANCE

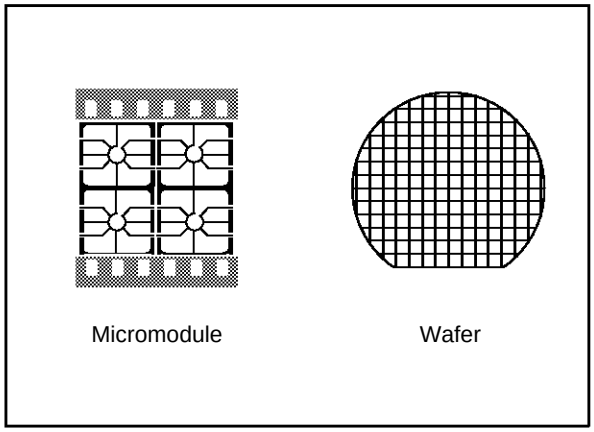
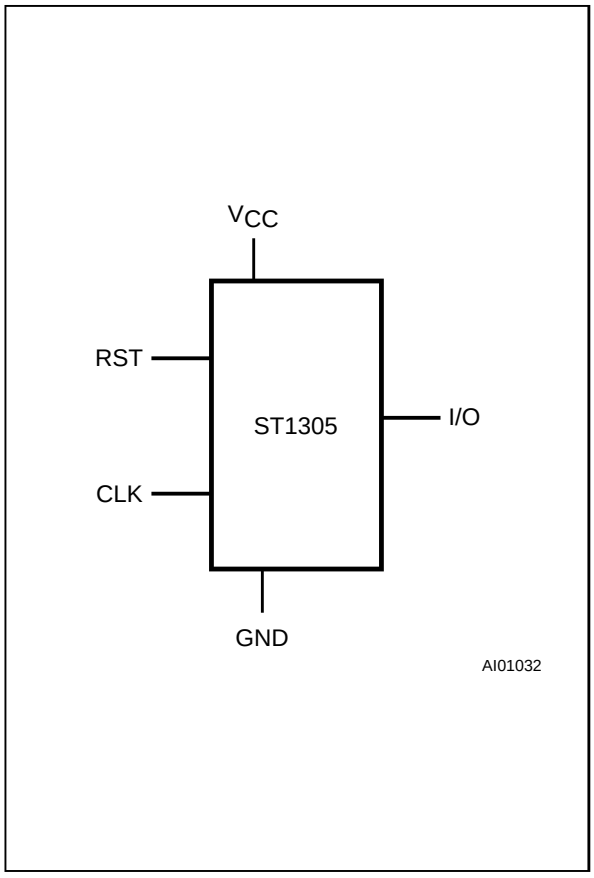


Figure 1. Pin Connection



DESCRIPTION

The ST1305 is a 192 bits EEPROM memory with associated security logic to control memory access. The circuit includes counting capabilities and thus is very well adapted to prepaid card applications.

Table 1. Signal Names

CLK	Clock
RST	Reset
I/O	Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

Figure 2A. Contact Connections

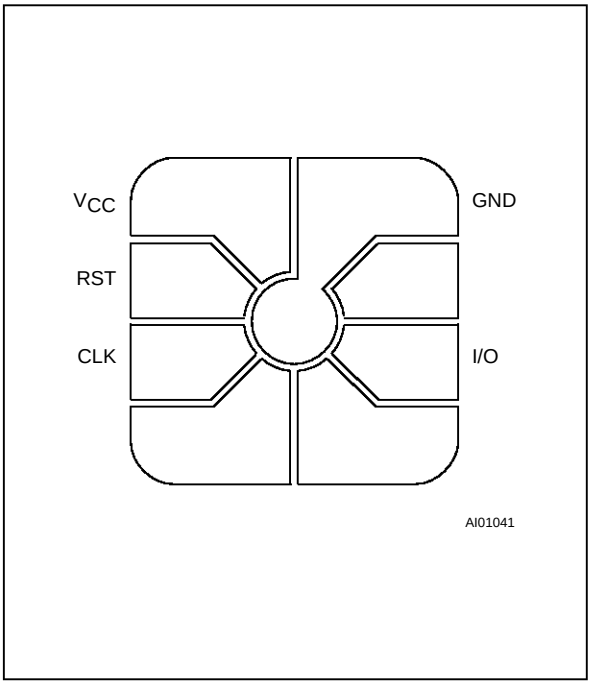


Figure 2B. Die Floor Plan

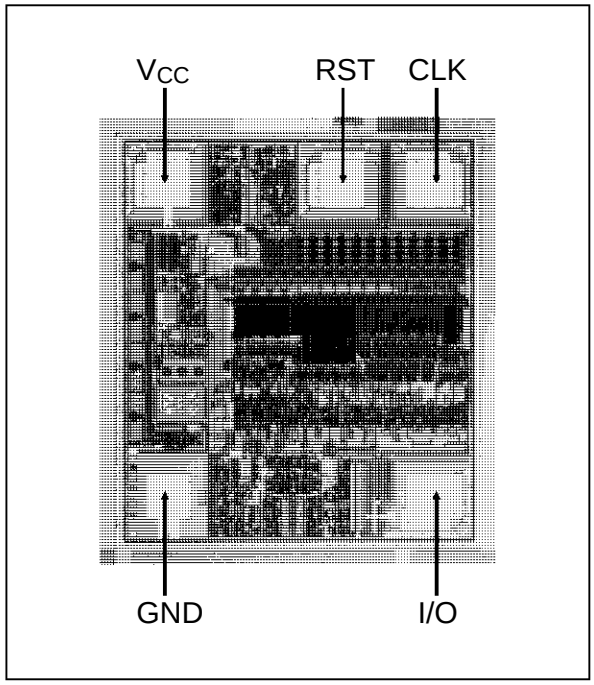


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–30 to 80	°C
T_{STG}	Storage Temperature	–55 to 125	°C
V_{IO} (1)	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
V_{CC} (2)	Supply Voltage Fuse Blow	6.65 to 7.35	V
V_{ESD} (3)	Electrostatic Discharge Voltage (Human Body model)	4000	V

Notes: 1. Not above V_{CC} + 0.3V
2. Only when Bit 262d = 1 and Bit 263d is being programmed for fuse blow.
3. MIL-STD-883 Method 3015-6

DESCRIPTION (Cont'd)

The ST1305 is protected by hardwired security logic and special fuses. The memory is a matrix of 24 x 8 cells accessed bit by bit for reading and programming, and by byte for internal erasing in final application.

This circuit receives 3 commands through external signals combination: RESET which resets the internal address to 00d, READ which increments the address and reads the corresponding data and finally, PROG which programs a bit at the current address. The circuit may be used in two different configurations, one for the card ISSUER, (card manufacturer) where special data may be written into the chip during initialisation, and another for the final USER configuration.

Before delivery, from SGS-THOMSON to the customer (the card issuer), the circuit is placed in the ISSUER configuration. This operation is performed by blowing the "test fuse".

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0V to 3V
Input Timing Reference Voltages	0.8V to 2V
Output Timing Reference Voltages	0.4V to 2.4V

Figure 3. AC Testing Input Output Waveforms

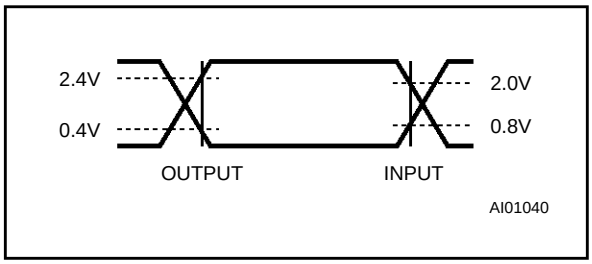


Figure 4. AC Testing Load Circuit

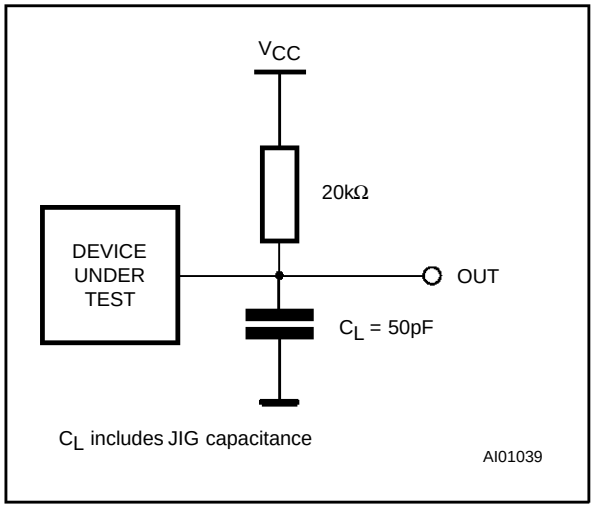


Table 3. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		10	pF

Note: 1. Sampled only, not 100% tested

Table 4. DC Characteristics (T_A = –30 to 80°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LO}	Output Leakage Current	V_{OH} = V_{CC}, Open Drain		10	µA
I_{CC}	Supply Current	CLK = '1'		5	mA
I_{CC1}	Supply Current (Standby)	CLK = '0'		500	µA
V_{IL}	Input Low Voltage	I_{IL} = ± 200µA	0	0.8	V
V_{IH}	Input High Voltage	I_{IH} = ± 500µA	2	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA	0	0.4	V

Table 5. AC Characteristics (T_A = –30 to 80°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Min	Max	Unit
t_{WW}	Spurious CLK or RST Pulse Width		100	ns
t_{WHR}	CLK Pulse Width (Read)	1.5		µs
t_{WLR}	Time Between CLK Pulses (Read)	1		µs
t_{WHW}	CLK Pulse Width (Program)	5		ms
t_{WLW}	Time Between CLK Pulses (Program)	3		µs
t_{WH}	RST Pulse Width (Set Program)	0.5		µs
t_{SR}	RST Stable Before CLK High	0.5		µs
t_{SC}	RST Stable After CLK Low	0.5		µs
t_{DZ}	Input Ouput Delay to Receive Mode		1	µs
t_{ZD}	Input Output Delay from Receive Mode	100		ns
t_{CC}	CODE Valid Before CKL Low	100		ns
t_{DVR} (1)	Output Valid After CLK Low (Read)		0.5	µs
t_{DVW} (1)	Output Valid After CLK Low (Program)		2.5	µs
t_{HRW}	Reset Stable After CLK Falling Edge	0.5		µs
t_{HRR}	Reset Hold Time After CLK Rising Edge	0.5		µs

Note: 1. Valid for transition from '1' to '0' only (Open Drain I/O).

Figure 5. Reset Mode AC Waveforms

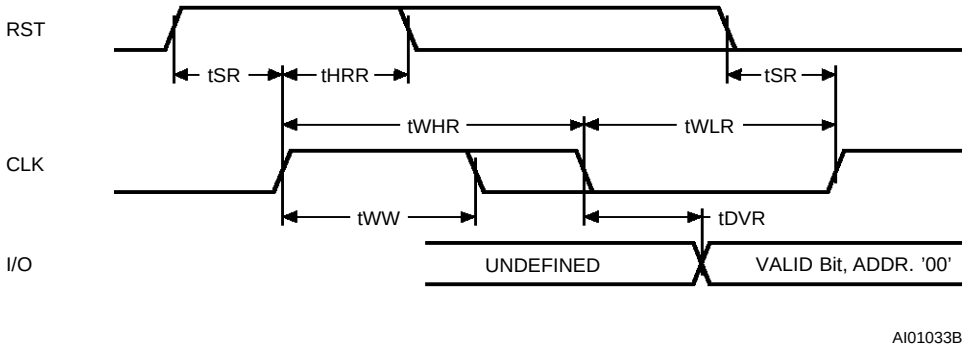


Figure 6. Read Mode AC Waveforms

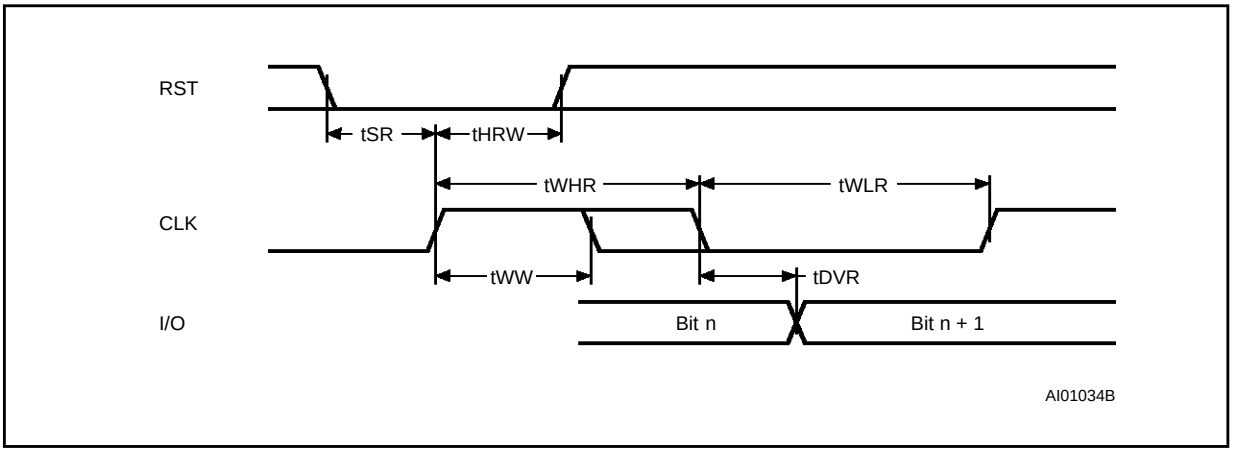


Figure 7. Program Mode AC Waveforms

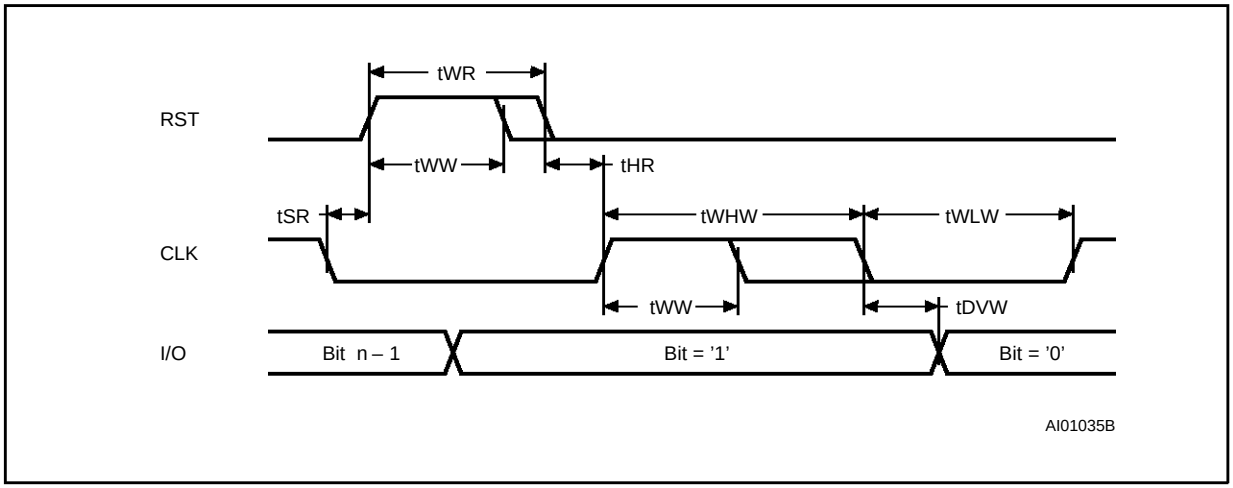
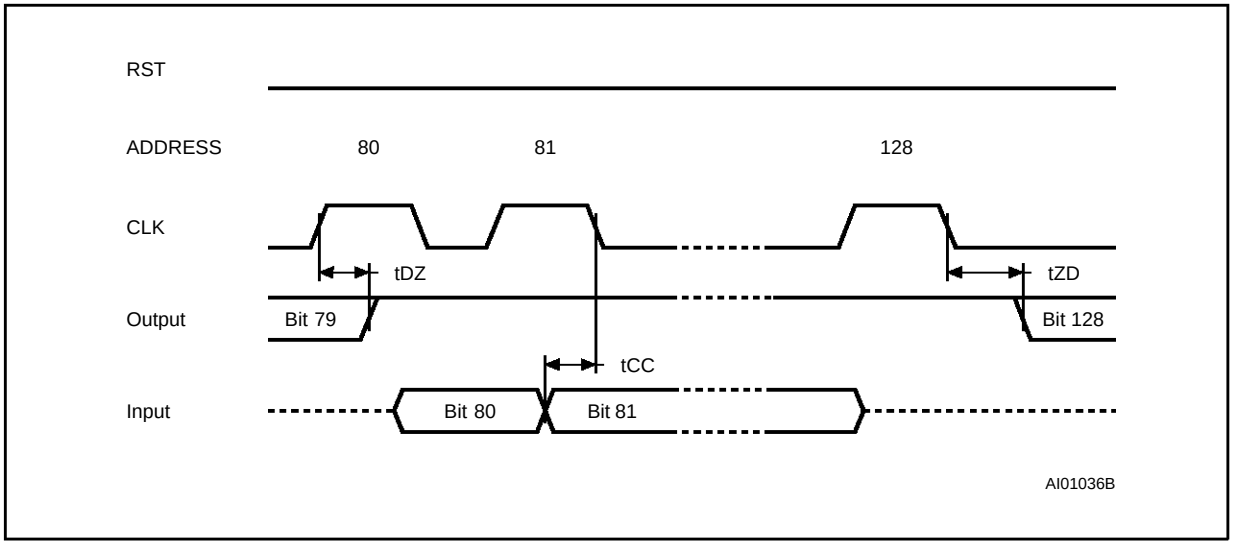


Figure 8. Issuer Configuration Presentation Waveforms



INTERNAL ADDRESS MAPPING

The internal address space of the ST1305 is divided into five zones as shown in Figure 9. These zones are the actual EEPROM memory array.

The Transport Code or Counter area is used in two configurations: In the ISSUER configuration it is used to store the Transport Code loaded by SGS-THOMSON for security during delivery to the card issuer; in the USER configuration it is used as a serie of counters. See Figure 10.

Circuit Identification Area (bit 00d to 15d). This area is programmed at factory level by SGS-THOMSON and contains information related to chip identification (type, manufacturer ...).

Bits 00d to 15d are mask programmed during wafer manufacturing. They are read only bits.

In the case of delivery in small quantity (including samples), bits 16d to 23d are programmed during product testing and cannot be altered after the chip has left the SGS-THOMSON plant. Read access to this area (bit 00d to 23d coded 0 1 1 ... 1 1) is allowed.

Application Identification Area (bit 16d to 63d). This area is programmed by the issuer and contains information on application and identification (serial number, application).

This area can only be programmed by the issuer if the correct Transport Code has been presented and validated. Once the ISSUER fuse has been programmed this area can no longer be programmed or erased. Read access is allowed.

Counter Area (bit 64d to 111d). This area, in USER configuration, is divided into 6 sub-counters as in Figure 10. To count units, the chip reader must write bits in counter 1A. When there are no more erased bits in counter 1A, writing 1B will enable the erasure of the 8 bits of counter 1A by a second PROG command. When both counters 1A and 1B are full, writing a bit in counter 2A will authorise the erasure of counter 1B by a second PROG command, and so on. Programming in counter 2B will authorise erasing of counter 2A, programming in 3A will authorise erasing in 2B and programming in 3B will authorise erasing in 3A. Counter 3B can never be erased.

This gives a counting capacity of 8^6 or 262,144 units. Preprogramming bits in counters will limit the total capacity. Not using the low order counter will also limit the capacity. For example, not using counter 1A would limit the counting capacity to 8^5 or 32,768 units.

Figure 9. Memory Map

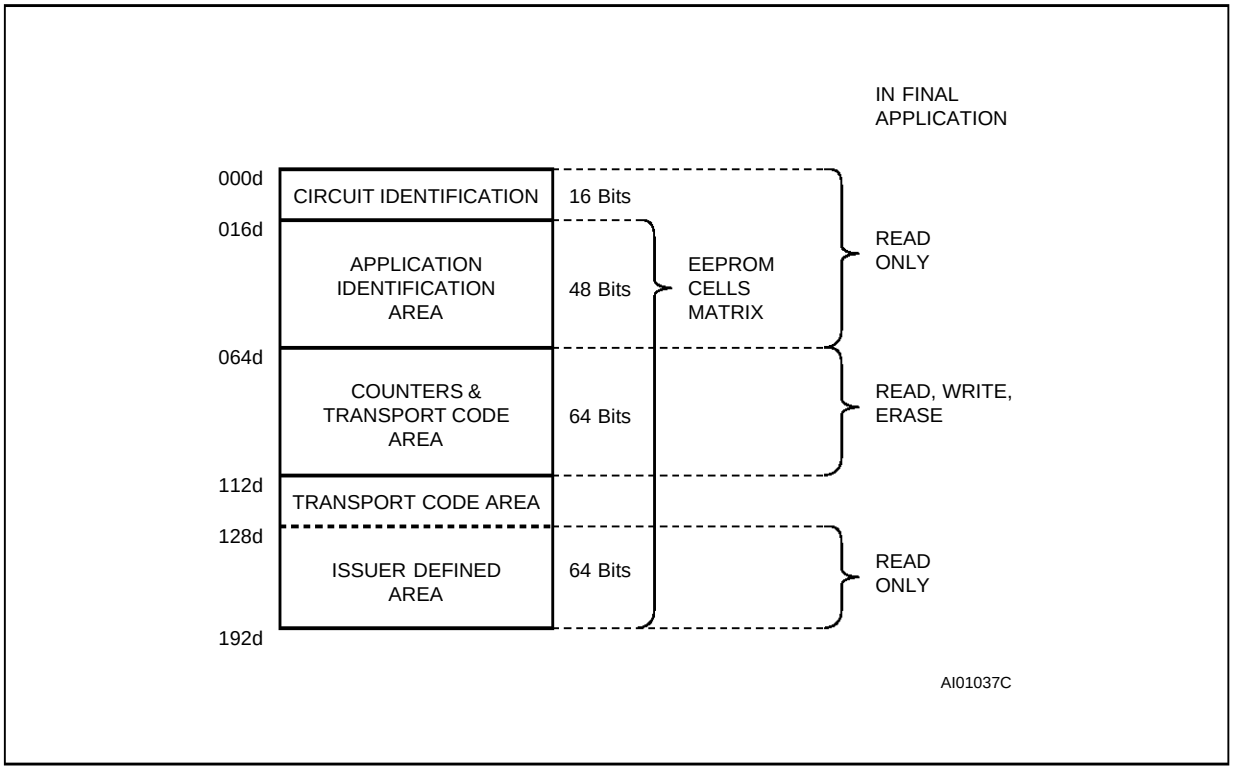


Table 6. Memory Access in Issuer Configuration

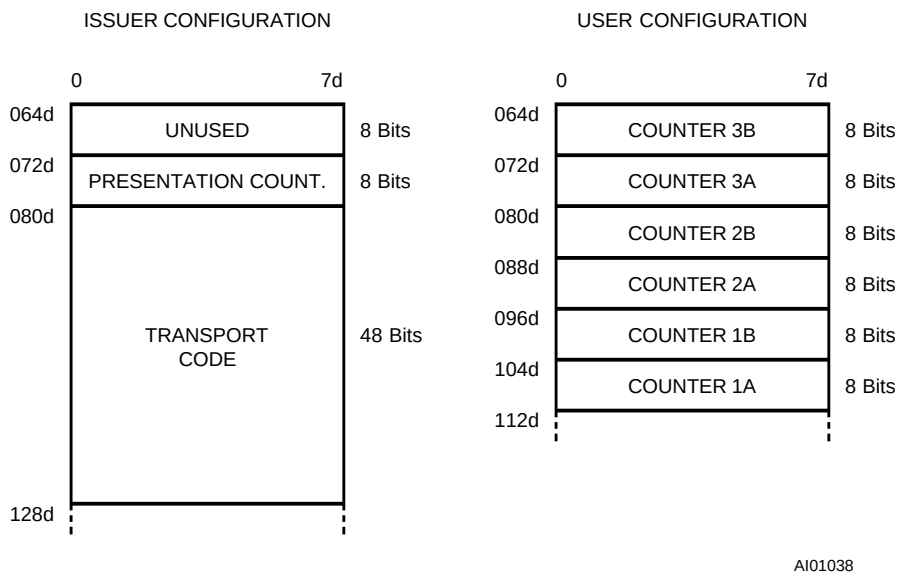
Memory Area	READ	WRITE	ERASE
Chip ID	Yes	No	No
Card ID	Yes	Yes if CODE OK	No
Counter 3B	Yes	No	No
Counter 3A	Yes	Yes	No
Counter 2B (2)	No (1)	No	No
Counter 2A (2)	No (1)	No	No
Counter 1B (2)	No (1)	No	No
Counter 1A (2)	No (1)	No	No
Transport Code 16 bit (2)	No (1)	No	No
Issuer Defined Area	Yes	Yes if CODE OK	No
Fuses	Yes	Yes if CODE OK	No

Notes: 1. Always READ as logic '0'.
2. Counters 2B to 1A and 16 bits past 1A contain a 48 bit Transport Code.

Table 7. Memory Access in User Configuration

Memory Area	READ	WRITE	ERASE
Chip ID	Yes	No	No
Card ID	Yes	No	No
Counter 3B	Yes	Yes	No
Counter 3A	Yes	Yes	Yes, by programming Counter 3B
Counter 2B	Yes	Yes	Yes, by programming Counter 3A
Counter 2A	Yes	Yes	Yes, by programming Counter 2B
Counter 1B	Yes	Yes	Yes, by programming Counter 2A
Counter 1A	Yes	Yes	Yes, by programming Counter 1B
Issuer Defined Area	Yes	No	No
Fuses	Yes	Yes	No

Figure 10. Issuer and User Memory Configuration



Transport Code Area (bit 80d to 127d). When the chip leaves SGS-THOMSON plant,

it is in the ISSUER configuration. In this mode, the counter area is configured as a Transport Code area. Counter area 3B is not used, counter 3A is used as code presentation counter. Counter 2B, 2A, 1B, 1A and following extra 16 bits contain a 48 bits transport code. Programming a bit in counter 3A (Bits 72d to 79d) will activate the code presentation mode allowing the comparison of bits presented on the I/O with bits programmed in the memory. Once the code if validated, card initialisation operations are allowed. After configuration in USER mode, it is necessary to program a bit in counter 3B (bit 64d for example) to allow erasure of the counters and the extra 16 bits area.

For security when attempting a read to this area, the circuit outputs '0' for all addresses.

Issuer Defined Area (bit 128d to 191d). This area can be programmed by the issuer and contains information on application and identification (serial number, application).

This area can only be programmed by the issuer if the correct transport code has been presented and validated. Once the ISSUER fuse has been programmed, this area can no longer be programmed or erased. Read access is allowed.

Security Fuses. As the ST1305 proceeds from SGS-THOMSON to the card ISSUER and to the user, security is maintained through the use of fuses which are read and blown by addressing the given locations. While the device is in the ISSUER configuration, programming access is denied until the Transport Code has been presented and validated. Following transport validation, the device may be set to USER configuration.

ACCESS IN ISSUER CONFIGURATION

When the chip is provided to the issuer, the memory access is set as ISSUER configuration, as explained in Table 6. Note that Counters 2B, 2A, 1B, 1A and an extra 16 bits area past 1A contain a 48 bits Transport Code (always read as '0').

ACCESS IN USER CONFIGURATION

Once the issuer has programmed all card data, programming the ISSUER fuse will set the chip in the USER configuration as shown in Table 7.

COMMANDS

In order to access the different areas described above, the circuit recognises three commands, provided through external signals RST and CLK.

RESET Command. The command is performed after sampling the RST line at a logic '1' on the rising edge of CLK. Data read on address 00d is then presented on the I/O line after the falling edge of CLK.

READ Command. A pulse applied on the CLK input will increment the address counter and read the corresponding bit in the memory array. Note than an erased bit is read as a logic '1' and a programmed one is read as a logic '0'.

PROG Command. To program a bit, it must first be addressed by repeatedly using the READ command and if the bit is erased, a pulse on the RST line will select the programming mode without changing the address counter. The next pulse applied on CLK will perform the programming of this bit.

Within the counter area, programming a bit may authorise the erasing of part of the counter. In that case if the programmed bit is verified (as being correctely programmed after the PROG command), then a second PROG command immediatly following the previous one, will cause the erasure of the required bits. If the read bit is not initially erased the PROG command will have no effect. If the verification after programming gives the wrong result (i.e. '1'), the second PROG command will not cause any erasure.

Data on I/O is irrelevant after the falling edge on CLOCK of the second PROG command.

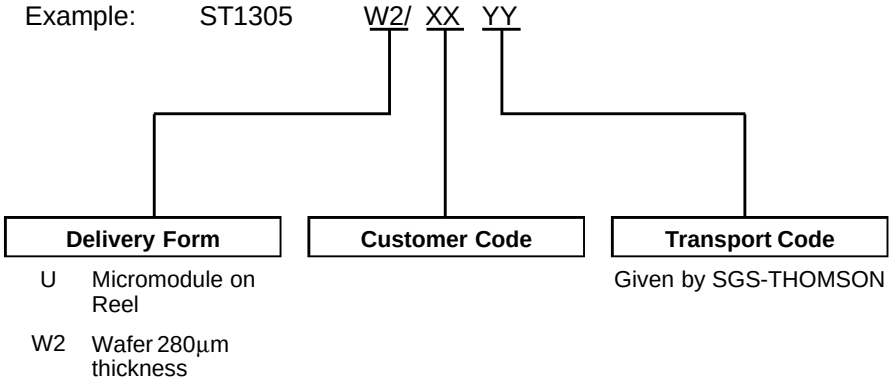
TRANSPORT CODE PRESENTATION

In ISSUER configuration, addresses 080d to 128d are used to store a 48 bits Transport Code. To validate a code it is necessary to program and erased bits in counter 3A, and then to present on the I/O (in reception mode) bit by bit, the code from addresses 80d to 127d. A RESET Command during this operation would stop the validation. The reception mode allows the card reader to send data to be compared internally.

The code is only validated when the address switches from 127d to 128d.

As there are 8 bits in counter 3A, it is possible to try 8 code presentations.

ORDERING INFORMATION SCHEME



For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.